ABSTRACT OF THE DISCLOSURE

A multiprocessor system including a master processor, a plurality of processor elements, each of which is provided with a local memory, the processor elements being controlled in accordance with commands from the foregoing master processor, and a global memory shared by the plurality of processor elements is disclosed. The processor elements are provided with a command pooling buffer capable of accumulating a plurality of commands, respectively. DMA controllers are also provided with a command pooling buffer capable of accumulating a plurality of commands, respectively. The master processor persistently issues a plurality of commands to the DMA controller and each processor element. A counter array manages the number of the issued commands which have received no response. When the responses are returned with respect to all issued commands, the counter array notifies the master processor of this.